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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,131	09/27/2000	Gary S. Kitten	M-8847 US	7081

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,131	KITTEN ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-10 and 13-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-10 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 3rd of January 2005. Claims 1, 2, 8 and 9 have been amended; no claim has been canceled; and no claim has been newly added since the RCE(2) Non-Final Office Action was mailed on 8th of October 2004. Currently, claims 1-3, 6-10 and 13-15 are pending in this application.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-3, 6-10 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phu et al. [US 6,321,278 B1; hereinafter Phu] in view of what was well known in the art, as exemplified by Jones et al. [US 4,776,203].

Referring to claim 1, Phu discloses an apparatus (i.e., computer system in Figs. 1A and 1B) comprising: a first audio input/output (I/O) connector (i.e., line-out jack 500 of Fig. 5) provided for coupling to a first audio I/O device (i.e., external loudspeakers 104 in Fig. 1A; See col. 7, lines 60-62); a second audio I/O connector (i.e., headphone jack/switch 405 of Fig. 5) provided for coupling to a second audio I/O device (i.e., headphone 106 of Fig. 1A; See col. 6, lines 35-38); said first and second connectors (i.e., line-out jack and headphone jack/switch) being coupled to an audio controller (i.e., coupled to Sound Device 116 in Fig. 5; See col. 9, lines 11-12) by a circuit (i.e., by a circuit including audio switch 220, unity gain amplifier 510, lines 418, 420, 520, 522, and resistor 404, 414, etc. in Fig. 5); and means for reducing noise (i.e., transistor switch 412 connected to voltage and ground in Fig. 5) coupled onto said first I/O connector (i.e., line-out jack) and limiting such noise (i.e., a sound signal from said line-out jack to said external loudspeakers, viz., unwanted sound signal to said loudspeakers) from interfacing with a signal from said second audio I/O connector (i.e., a sound signal from said headphone jack/switch to said

headphone, viz., desired sound signal to said headphone), and said means for reducing noise including a transistor (i.e., transistor switch 412 of Fig. 5) coupled to said first and second connectors and to ground (See Fig. 5 and col. 5, lines 51-65), said transistor (i.e., transistor switch) connected to pull said first device (i.e., external loudspeakers) coupled to said first I/O connector (i.e., line-out jack) to a zero voltage level (i.e., a logic "0") when said second device (i.e., headphone) is coupled to said second I/O connector (i.e., headphone jack/switch; See col. 5, line 66 through col. 6, line 7 and lines 35-60).

Phu does not expressly teaches said transistor is a field effect transistor.

The Examiner takes Official Notice that a field effect transistor being used as a transistor for switching connection (i.e., short circuit or removing said short circuit operations), is well known to one of ordinary skill in the art, as evidenced by Jones (See FET 20 of Fig. 1 and col. 3, lines 50-68).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used said field effect transistor (i.e., FET) as said transistor (i.e., transistor switch) since it would have provided a cheaper and simpler arrangement for manufacturing because said field effect transistor (i.e., FET) could be built into a printed circuit board simply (See Jones, col. 2, lines 13-17).

Referring to claim 2, Phu teaches a PCI bus (i.e., Primary PCI Bus 12 of Fig. 1B) connecting a PCI card slot (i.e., means for connecting Primary Memory Controller/Bridge 160 to said Primary PCI Bus 12 in Fig. 1B) to a card/bus controller (i.e., Primary Memory Controller/Bridge 160 of Fig. 1B; in fact, said Primary Memory Controller/Bridge connecting one or more buses such as Host Bus 144, Memory Bus 52, AGP Bus 16 in Fig 1B), said audio controller (i.e., Sound Device 116 of Fig. 5) connected to said PCI bus (i.e., said Sound Device 116 is connected to said Primary PCI Bus 12 via PCI/ISA Bridge 20 in Fig. 1B; See col. 3, lines 44-47), and an I/O controller hub (i.e., PCI/ISA Bridge 20 of Fig. 1B) connected to said PCI bus (i.e., said PCI/ISA Bridge 20 is connected to said Primary PCI Bus 12 in Fig. 1B).

Referring to claim 3, Phu teaches a super I/O controller (i.e., Super I/O device 40 of Fig. 1B) connected to said I/O controller hub (i.e., said Super I/O device 40 being connected to said PCI/ISA Bridge 20 in Fig. 1B; See col. 3, lines 44-47).

Referring to claim 6, Phu teaches said first audio I/O connector comprises a jack (i.e., line-out jack 500 of Fig. 5).

Referring to claim 7, Phu teaches said second audio I/O connector comprises a jack (i.e., headphone jack/switch 405 of Fig. 5).

Referring to claim 8, Phu discloses a computer system (i.e., computer system in Figs. 1A and 1B) comprising: a processor (i.e., Processor 10a of Fig. 1B); a memory (i.e., Primary Memory 164 of Fig. 1B) coupled to said processor (i.e., said Primary Memory 164 being coupled to said Processor 10a via Primary Memory Controller/Bridge 160 in Fig. 1B); an audio controller (i.e., Sound Device 116 of Fig. 1B; See col. 9, lines 11-12) coupled to said processor (i.e., said Sound Device 116 being coupled to said Processor 10a via PCI/ISA Bridge 20 and Primary Memory Controller/Bridge 160 in Fig. 1B); a first audio input/output (I/O) connector (i.e., line-out jack 500 of Fig. 5) coupled to said audio controller (i.e., said line-out jack 500 being coupled to said Sound Device 116 in Fig. 5) and provided for coupling to a first audio I/O device (i.e., external loudspeakers 104 in Fig. 1A; See col. 7, lines 60-62); a second audio I/O connector (i.e., headphone jack/switch 405 of Fig. 5) coupled to said audio controller (i.e., said headphone jack/switch 405 being coupled to said Sound Device 116 in Fig. 5) and provided for coupling to a second audio I/O device (i.e., headphone 106 of Fig. 1A; See col. 6, lines 35-38); and a transistor (i.e., transistor switch 412 of Fig. 5) coupled to said first and second connectors and to ground (See Fig. 5 and col. 5, lines 51-65), said transistor (i.e., transistor switch) connected to pull said first device (i.e., external loudspeakers) coupled to said first I/O connector (i.e., line-out jack) to a zero voltage level (i.e., a logic "0") when said second device (i.e., headphone) is coupled to said second I/O connector (i.e., headphone jack/switch; See col. 5, line 66 through col. 6, line 7 and lines 35-60), said transistor functioning as a

means for reducing noise (i.e., transistor switch 412 being connected to voltage and ground in Fig. 5 for on/off control of unwanted signals) coupled onto said first I/O connector (i.e., line-out jack) and limiting such noise (i.e., a sound signal from said line-out jack to said external loudspeakers, viz., unwanted sound signal to said loudspeakers) from interfacing with a signal from said second audio I/O connector (i.e., a sound signal from said headphone jack/switch to said headphone, viz., desired sound signal to said headphone).

Phu does not expressly teaches said transistor is a field effect transistor.

The Examiner takes Official Notice that a field effect transistor being used as a transistor for switching connection (i.e., short circuit or removing said short circuit operations), is well known to one of ordinary skill in the art, as evidenced by Jones (See FET 20 of Fig. 1 and col. 3, lines 50-68).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used said field effect transistor (i.e., FET) as said transistor (i.e., transistor switch) since it would have provided a cheaper and simpler arrangement for manufacturing because said field effect transistor (i.e., FET) could be built into a printed circuit board simply (See Jones, col. 2, lines 13-17).

Referring to claim 9, Phu teaches a PCI bus (i.e., Primary PCI Bus 12 of Fig. 1B) connected to a PCI card slot (i.e., means for connecting Primary Memory Controller/Bridge 160 to said Primary PCI Bus 12 in Fig. 1B) to a card/bus controller (i.e., Primary Memory Controller/Bridge 160 of Fig. 1B; in fact, said Primary Memory Controller/Bridge connecting one or more buses such as Host Bus 144, Memory Bus 52, AGP Bus 16 in Fig 1B), said audio controller (i.e., Sound Device 116 of Fig. 5) connected to said PCI bus (i.e., said Sound Device 116 is connected to said Primary PCI Bus 12 via PCI/ISA Bridge 20 in Fig. 1B; See col. 3, lines 44-47), and an I/O controller hub (i.e., PCI/ISA Bridge 20 of Fig. 1B) connected to said PCI bus (i.e., said PCI/ISA Bridge 20 is connected to said Primary PCI Bus 12 in Fig. 1B).

Referring to claim 10, Phu teaches a super I/O controller (i.e., Super I/O device 40 of Fig. 1B) connected to said I/O controller hub (i.e., said Super I/O device 40 being connected to said PCI/ISA Bridge 20 in Fig. 1B; See col. 3, lines 44-47).

Referring to claim 13, Phu teaches said first audio I/O connector comprises a jack (i.e., line-out jack 500 of Fig. 5).

Referring to claim 14, Phu teaches said second audio I/O connector comprises a jack (i.e., headphone jack/switch 405 of Fig. 5).

Referring to claim 15, Phu teaches said first connector (i.e., line-out jack 500 of Fig. 5) and said second audio I/O connector (i.e., headphone jack/switch 405 in Fig. 5), each comprise a jack (i.e., combination jack; See Abstract).

Response to Arguments

4. Applicant's arguments filed on 3rd of January 2005 with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
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